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Application No. 09/619,123

Filed: July 19, 2000

TC Art Unit: 3737

Confirmation No.: 1997

REMARKS

Claims 75-77 and 87-94 have been rejected under 35 U.S.C. 103(a) as being obvious over Daigle in view of Shinomura and Mallart. Claims 78-80, 82, 84 and 85 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Daigle in view of Shinomura and Mallart, and further in view of Blackwell.

Claim 75 has been amended, without prejudice to the filing of continuation and/or divisional applications, to recite a programmable beamforming integrated circuit. Claim 75 has been further amended to recite that the integrated circuit is connected to a control circuit that controls a variable delay setting of the beamforming integrated circuit. Claims 78 and 87 have also been amended without prejudice to recite the integrated circuit beamforming architecture in a light weight device.

Shinomura specifically teaches that the "signal processing units 27A and 27B ... may be structured so as to be applied to several ultrasonic scanning modes such as linear electronic scanning, convex electronic scanning ... But this increases their circuit scale so that in the present invention, they are structured so as to be applied to a specific ultrasonic scanning mode, respectively. Thus, the main systems 2A and 2B ... can be simplified in circuit configuration, made small in size and light in weight ..." (Column 8, lines 49-59). Although Shinomura fails to

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describe in any detail the beamforming device used in the operation of the device in Fig. 3, it is clear from this description that the circuitry in this device is configured to work with only one scanning mode (see also Shinomura at column 10, lines 16-18). The present invention solves this problem by providing an integrated circuit beamformer having at least 10 channels that is programmable, that is, in which the delay applied by the beamformer is variable or adjustable and can thus be configured to accommodate different scanning modes.

The Daigle reference also fails to teach or suggest such a structure. Figure 9 of Daigle shows a 3 channel delay device with separate data memories 211, 212, 213. There is no teaching that this delay device employs a variable delay integrated circuit architecture. There is no disclosure or suggestion in Daigle that the delay device can have at least 10 channels in a single integrated circuit. Shinomura also certainly fails to describe an integrated circuit beamformer having either 10 or 64 channels as now recited in claims 75, 78 and 87. Note further that the only signal processing functions carried out by the system in Shinomura (Figs. 3 and 4) is described at column 10, lines 31-43. This does not include scan conversion or Doppler processing. Additional processing is carried out using a memory card 4A to transfer the data to a larger system. Thus, the present invention, by reducing

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the size and weight of the beamforming architecture, provides for increased processing capability in a light weight system. Also, claim 95 has been added reciting a memory that stores beamforming control signals (see Figs. 4, 7-11, 13, 14A, 15-22 and 27 for embodiments thereof). The cited references fail to disclose or suggest such a structure.

The Mallart, Cannon, Blackwell, Dubil and Wilson references are also silent as to how to implement a beamforming ultrasound system having these numbers of channels and yet the reduced weight as set forth in the claims and at the same time the processing capability for scan conversion/Doppler processing for the images created by such a system.

Reconsideration of the claims is respectfully requested.

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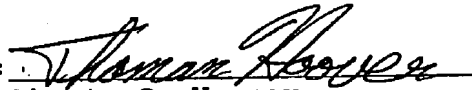
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The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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